# UNITED STATES PATENT AND TRADEMARK OFFICE

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| 10/566,514 | 01/30/2006 | Gregory Goodhue | US03 0253 US2 | 6165 |

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| 65913          7590          06/19/2007 | | EXAMINER |
| NXP, B.V.<br>NXP INTELLECTUAL PROPERTY DEPARTMENT<br>M/S41-SJ<br>1109 MCKAY DRIVE<br>SAN JOSE, CA 95131 | | FONG, VINCENT |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>20 March 2007</u>.

2a)☒ This action is **FINAL**.          2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-6,8-11,14-16 and 18-21</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,2,8-11,15,16 and 18-21</u> is/are rejected.

7)☐ Claim(s) <u>3-6 and 14</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>01-30-2006</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the amendments filed on 03-20-2007.

Claims 1-6, 8, 10-11, 14-16 are amended.

Claims 7, 12-13 and 17 are cancelled.

Claims 18-21 are added.

Claims 1, 2, 8-11, 15-16 and 18-21 are rejected.

Claims 3-6 and 14 are objected.

Claims 1-6, 8-11,14-16 and 18-21 are pending and have been examined.

## *Claim Rejections - 35 USC § 112*

1.     The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2.     Claims 18-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 18, the specification does not provide support to the limitation of "fourth multiplexer that selectively provides a fourth multiplexer output that includes portions of data from the second multiplexer output and portions of data from the second block of memory".

Any claim not specifically addressed above, is being rejected as incorporating the

deficiencies of a claim upon which it depends.


3.      The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

4.      Claims 18-21 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Claim 18 recites the limitation "the plurality of pointer

registers" in line 11. There is insufficient antecedent basis for this limitation in the claim.

It is unclear whether the limitation is referring to first plurality of pointer registers or

second plurality of pointer registers or both.

Any claim not specifically addressed above, is being rejected as incorporating the

deficiencies of a claim upon which it depends.


## Claim Rejections - 35 USC § 102

5.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.

6.      Claims 1, 2, 8-11 and 15-16 are rejected under 35 U.S.C. 102(b) as being

anticipated by Broxterman et al. (USPN 6058467, hereinafter Broxterman).

As per claim 1, Broxterman discloses:

A microcontroller architecture comprising: a processor (element 24, figure 1) for

processing of instruction data comprising memory access instructions (Column 4, lines

19-29) for accessing of a memory circuit (element 402, figure 4); the processor

operationg responsive to a clock circuit for providing clock cycles (column 2 lines 20-

28); at least a pointer memory circuit (element 402, figure 4), the memory circuit stores

both pointer and regular data(figure 3), for storing of a pointer address forming part of

the instruction data; at least a pointer register (element 404, figure4) for storing a

duplicate of the pointer address(column 5 lines 32-36); and, a control circuit (element

rden, wren) for determining whether one of a read operation from the at least a pointer

memory circuit and a write operation to the at least a pointer memory circuit is to take

place, there are signals generated for read/write operation on the memory circuit, the

control circuit that generate such signals is inherent exists, wherein the clock circuit is

coupled to the at least a memory circuit (element 402 figure 4), the at least a pointer

register (element 404 figure 4) and the control block (element 414 figure 4), and the

read operation accesses a region in the memory circuit that is addressed by the target

pointer address within a single cycle of determining a read operation is to take place

(after decoding the indirect access instruction, the address is read from the shadow

registers then pass through two muxes to access the memory, since muxes are

combinational, they do not take up clock cycle therefore the access to the memory can

begin within a cycle of the decode,figure 4), wherein for a write operation the control

circuit  stores the pointer address in the at least a pointer memory circuit and

automatically stores a duplicate in the at least a pointer register (column 5 lines 44-

51)and where for a read operation the control circuit utilizes the at least a pointer

register to access data pointed to by a target pointer address derived from the pointer

address stored therein without accessing the at least a pointer memory (column 6 lines

4-26).

As per claim 2, rejection of claim 1 is incorporated and Broxterman further discloses:

A microcontroller architecture according to claim 1, comprising a pointer multiplexer

block  (element 418, figure 4) having at least an input port coupled to the at least a

pointer register for receiving a pointer address and an output port for providing the

pointer target address used for indirect addressing operations of data stored within the

memory circuit.

As per claim 8, Broxterman discloses:

A method of pointer based addressing comprising the steps of: providing at least a

pointer memory (element 402 figure 4); providing at least a pointer register (element

404 figure 4); storing of a pointer address data in the at least a pointer memory; and,

upon storing of a pointer address data in the at least a pointer memory, automatically

storing a duplicate pointer address data, which is a duplicate of the pointer address

data, in the at least a pointer register (column 5 lines 46-52, 60-62); receiving a memory

access request to a memory location within a memory for retrieving of data stored at the

memory location addressed by the pointer address(column 5 lines 4-5); retrieving of the

duplicate pointer address data from the pointer register (column 6 lines 7-10); and,

accessing the memory using a target pointer address derived from the duplicate pointer

address data without using a target pointer address derived from the pointer address

data stored in the at least a pointer memory (column 6 lines16-20), wherein the steps of

retrieving and accessing occur within one clock cycle of receiving (after decoding the

indirect access instruction, the address is read from the shadow registers then pass

through two muxes to access the memory, since muxes are combinational, they do not

take up clock cycle therefore the access to the memory can begin within a cycle of the

decode,figure 4).

As per claim 9, rejection of claim 8 is incorporated and Broxterman further discloses:

the step of automatically storing is performed within a same clock cycle as the step of

storing (column 5 lines 46-52).

As per claim 10, rejection of claim 8 is incorporated and Broxterman further discloses:

the step of automatically storing is performed after the step of storing (column 5 lines

46-52), writing to memory trigger the write in the shadow copy, such that the at least a

pointer memory is not accessible by other operations until the step of automatically

storing is completed; both acts of storing would complete at the same cycle which no

other operation would be issued to access the memory.

As per claim 11, rejection of claim 8 is incorporated and Broxterman further discloses:

A method according to claim 8 comprising the step of detecting all changes to the at

least a pointer memory for automatically storing the duplicate pointer address data

(column 5 lines 41-44, 46-52).

As per claim 15, rejection of claim 8 is incorporated and Broxterman further discloses:

the step of detecting all changes to the at least a pointer memory for automatically

storing the duplicate pointer address data (column 5 lines 41-44, 46-52).

As per claim 16, rejection of claim 8 is incorporated and Broxterman further discloses:

the at least a pointer register comprises a plurality of pointer registers (element 404

figure 4), wherein the step of accessing comprises the step of multiplexing of the pointer

address data (element 418 figure 4) stored in the plurality of pointer registers to form the

target pointer address for accessing of the random access memory (column 6 lines16-

20).

## Response to Arguments

5.     Applicant's arguments filed 03-20-2007 have been fully considered. Argument (1)

is not persuasive. Argument (2) is persuasive. In remarks, the applicant argues in

substance:

(1) Applicant argues that Broxterman reference fails to teach each of the claimed

limitation in claims 1 and 8 in particular completing the read operation in a single cycle.

(2) Applicant argues that there are lack of adequate motivation to do the combination

asserted in the rejection of claim 3, 4, 6 and 14.

Response

(1) The limitation of operation being performed in a single clock cycle is not in the

original nor amended claim 1 and 8. The limitation incorporated in the amended claim 1

and 8 is "the read operation accesses a region in the memory circuit that is addressed

by the target pointer address within a single cycle of determining a read operation is to

take place". Examiner interprets the claim limitation as after the determination of a read

operation to take place (decode of instruction), the read operation to the region of

memory pointed by the pointer is initiated within a single cycle. It is not necessary to

complete the read operation in a single cycle.

(2) Examiner recognize the motivation of combination in rejection of claims 3, 4, 6 and

14 is inadequate.


*Allowable Subject Matter*

6.      Claims 3-6 and 14 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

7.      The following is a statement of reasons for the indication of allowable subject

matter:  Prior art does not teach or suggest "a source select block having a first input

port for receiving a next program address derived from a current program counter value plus a length of a current instruction, a second input port for receiving the pointer target address from the pointer multiplexer block, a third input port for receiving a selection signal from the control circuit for determining which data bits from the at least one of the input signals received at the first and second input ports are to be used for providing of pointer data output signals from output ports of the source select block" as found in claim 3.

Prior art does not teach or suggest "writing back the target pointer address to the at least a pointer register and to the at least a pointer memory" as found in claim 14. Prior art does not teach the write back of target pointer address.

### *Conclusion*

8.      Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**  See MPEP § 706.07(a).  Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action.  In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of
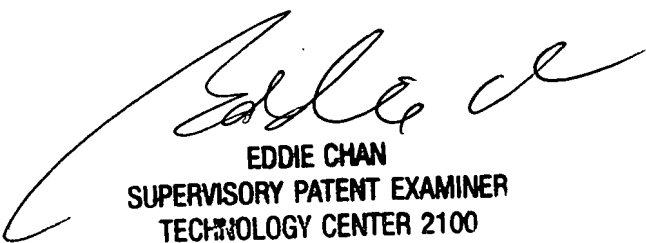
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on 7:00-3:30 Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VF
Vincent Fong
June 9 2007

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